Next Generation Energy Efficient Smart Transistor: From Transport Phenomena to Integrated Circuit Design

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1ST EECS GSRS 2017

Introduction

The Moore's law of scaling of metal oxide field effect transistors (MOSFET) resulted an unprecedented advancement in technology over the last five decades, until recently chips are now down for Moore's law.

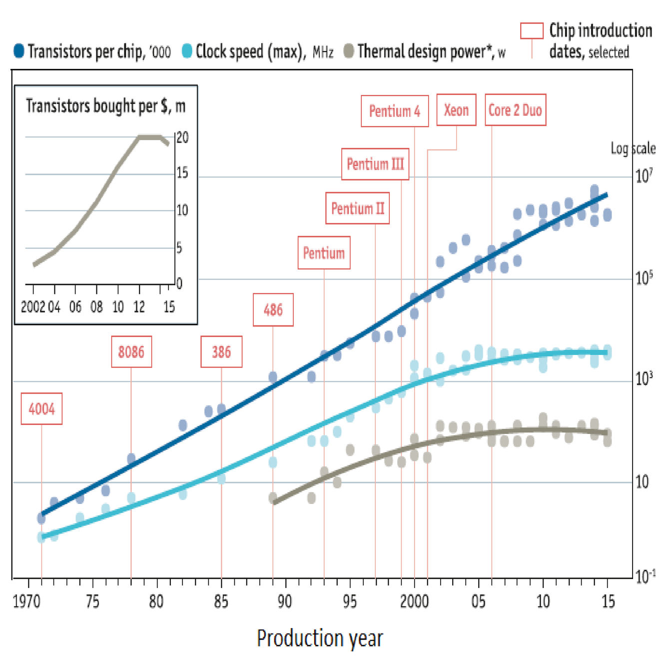


Fig. 1. MOSFET scaling trend and transport phenomena

Quantum mechanical band to band tunneling transport overcomes fundamental physical limit of MOSFET for supply voltage scaling, resulting **energy efficient smart transistor technology**.

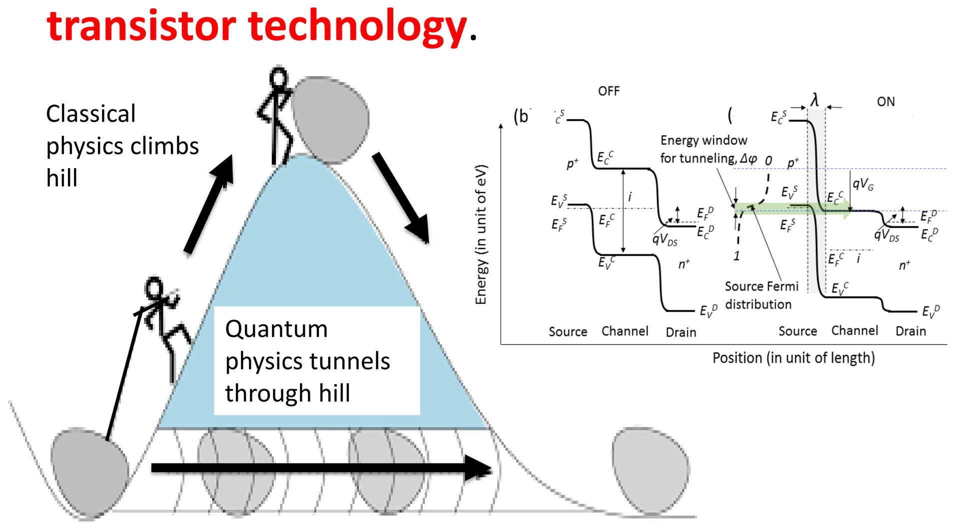


Fig. 2. Quantum tunneling transport phenomena in FET

Goals

1. Model current transport in novel smart tunneling transistors from atomically thin two dimensional (2D) materials for:
   - Operates at low supply voltage (~ 0.1V)
   - THz operation and fs delay
2. Incorporate models for circuit simulations.

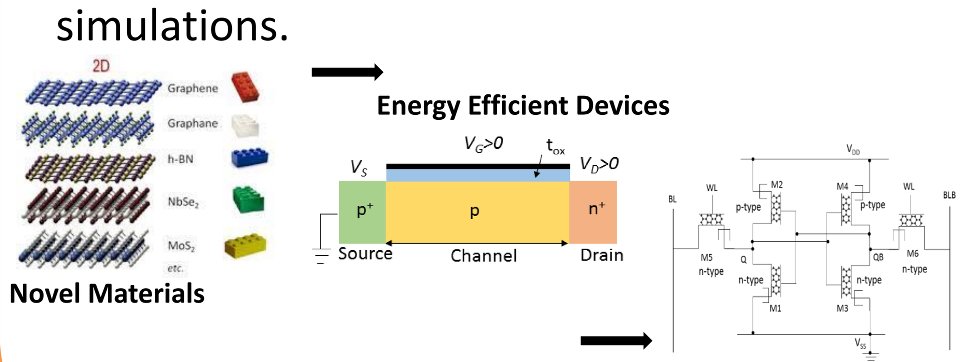
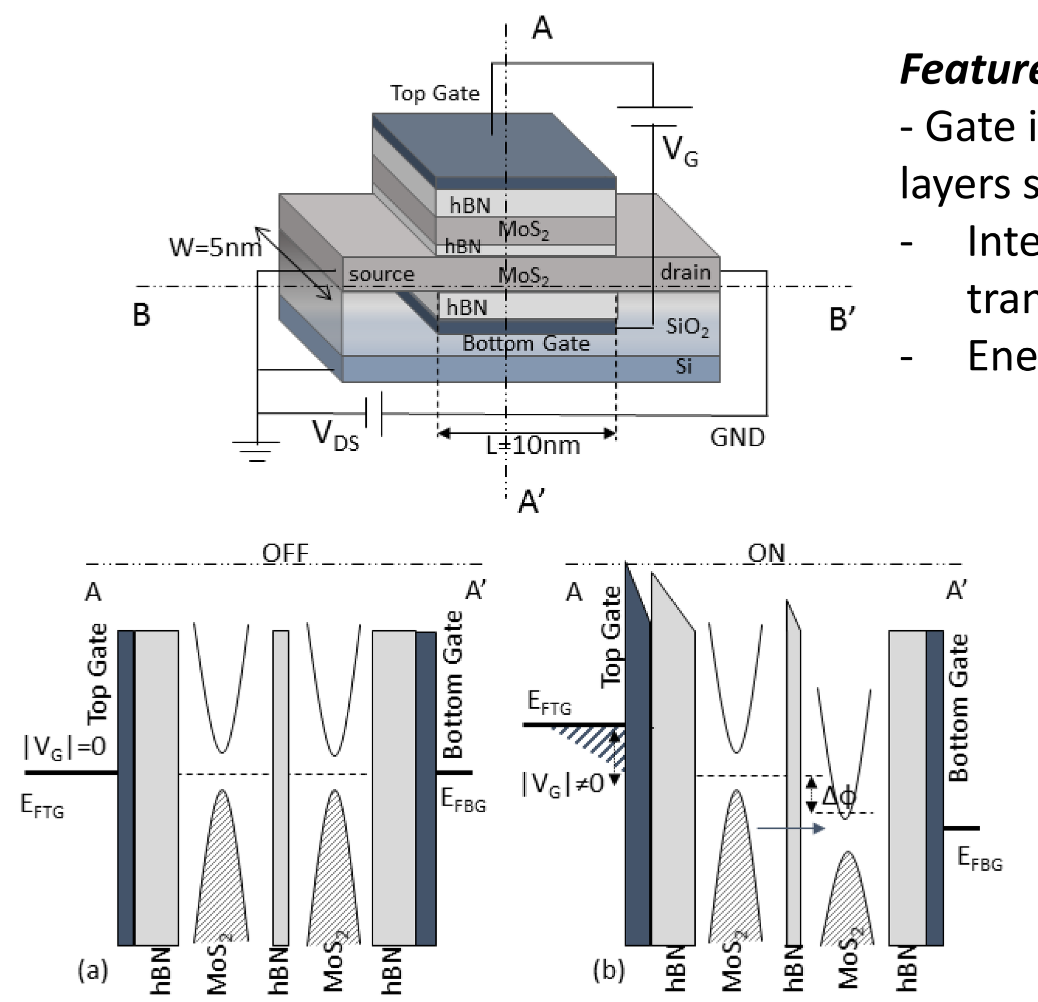


Fig. 3. From material modeling to circuit design

Device Transport Modeling and Performance

MoS_2-hBN-MoS_2 Junctionless Tunnel Effect Transistor



Features:

- Gate induced interlayer tunneling between two MoS_2 layers separated by hBN changes channel charge density.
- Interlayer tunneling controls the source-drain ballistic transport.
- Energy efficient high speed THz operation.

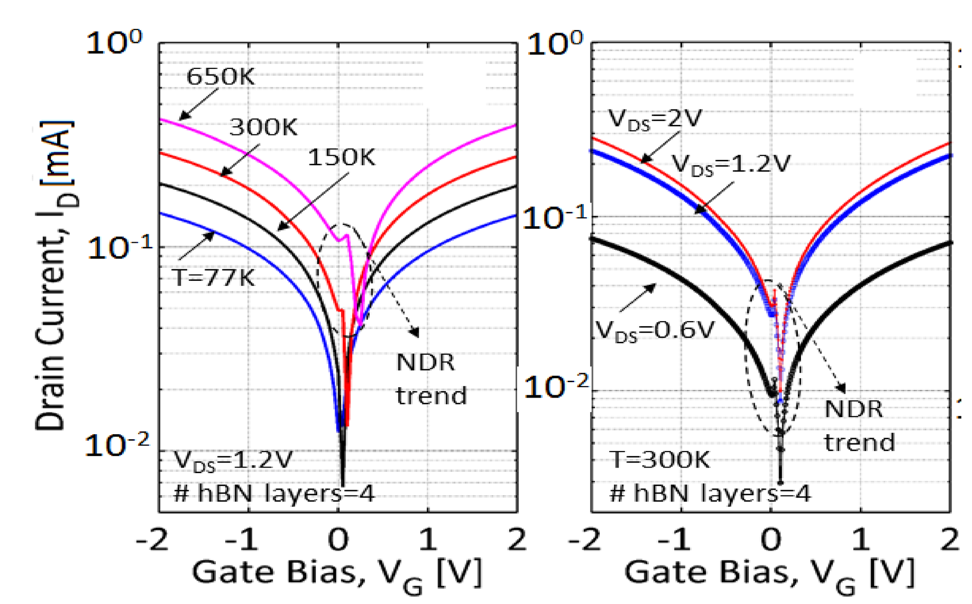
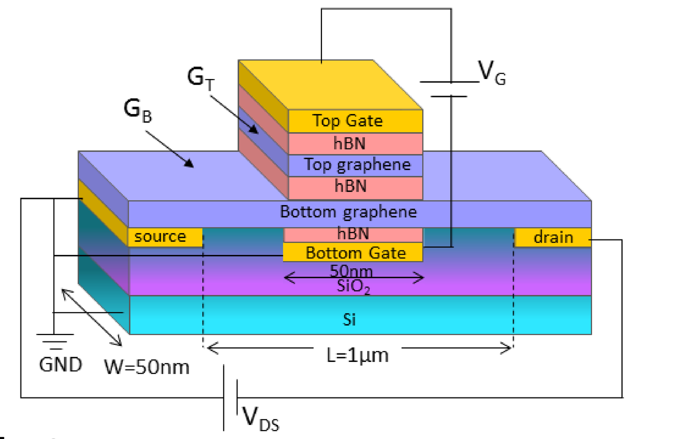
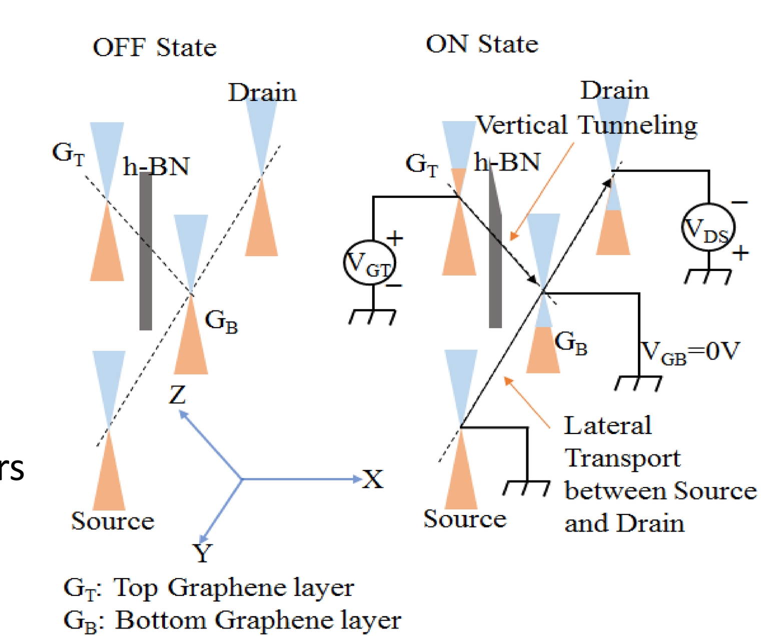


Fig. 4. Junctionless tunnel effect transistor: device structure, current transport, charge induced barrier control mechanism and high speed performance at ultra-low delay operation

Graphene-hBN-Graphene Junctionless Tunnel Effect Transistor





Features:

- Tunneling between two graphene layers separated by hBN.
- Low supply voltage operation
- Steep subthreshold slope
- Current ratio of 10^4 with mA range On-current

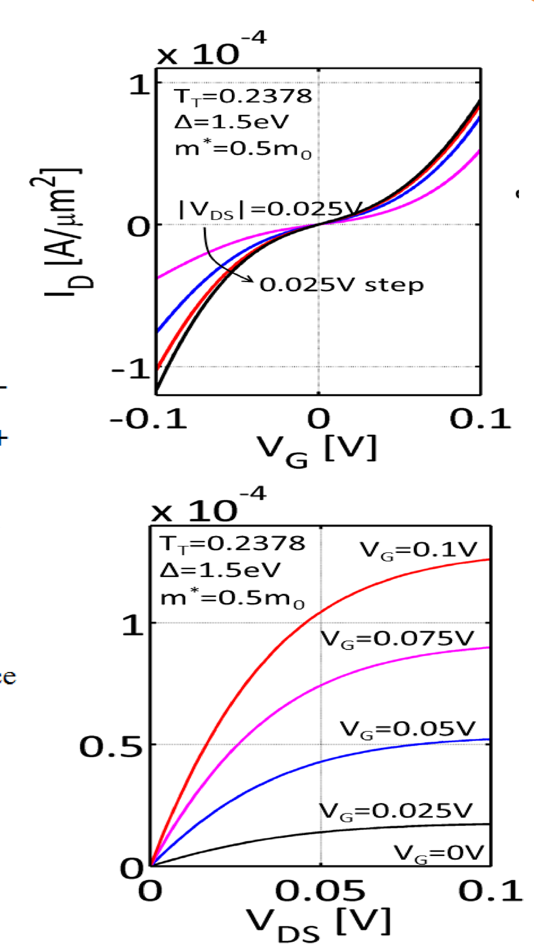


Fig. 5. Junctionless graphene tunnel effect transistor with steep subthreshold slope operation

Graphene and Silicene Nanoribbon Tunnel Effect Transistor

Features:

- Width tuable energy band gap in graphene and silicene nanoribbon.
- Suitable for logic application.
- High mobility, high on/off current ratio and ultra-low power (pW) operation

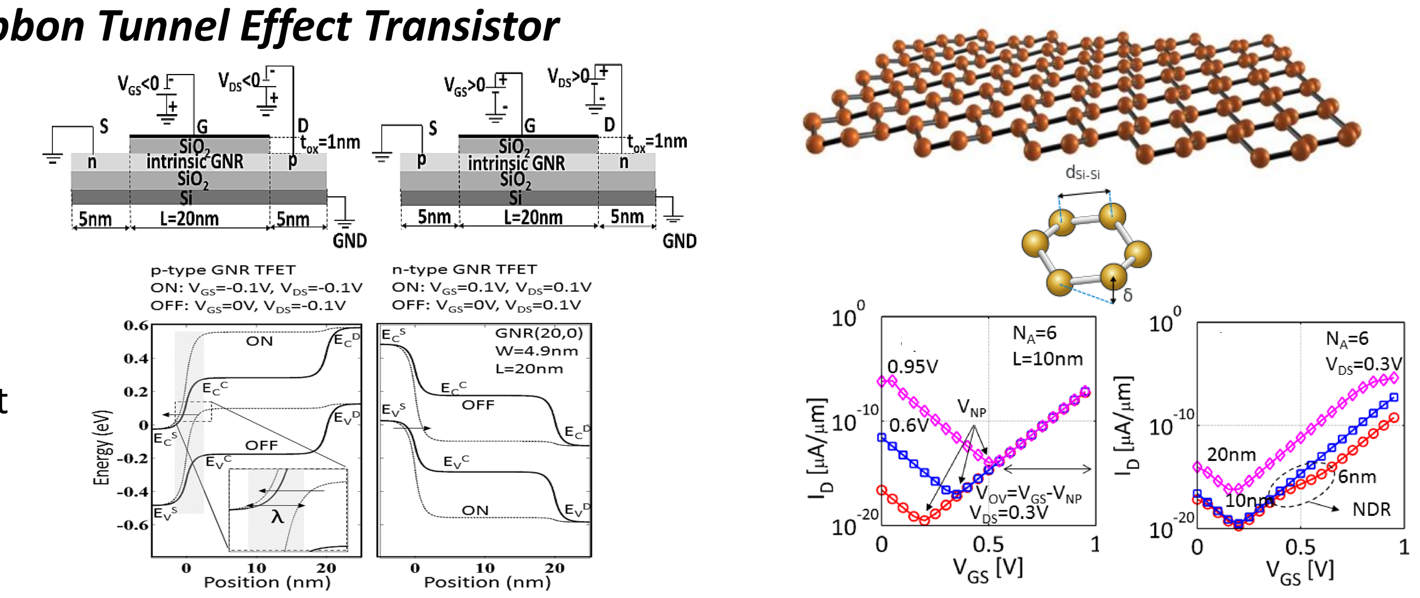
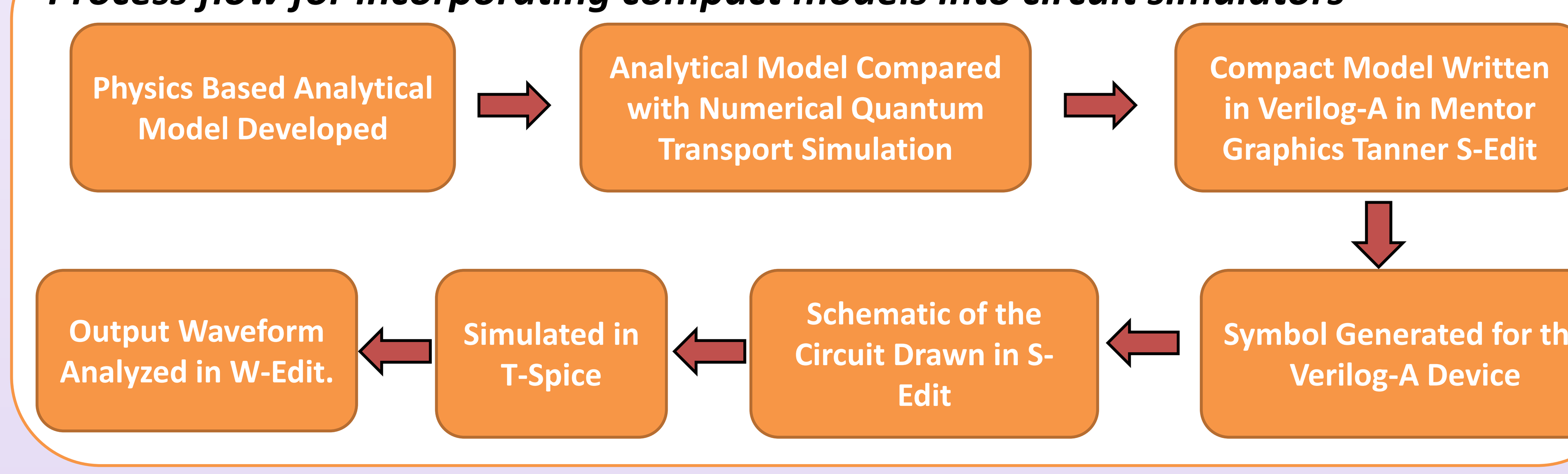


Fig. 6. Quantum transport simulation of graphene and silicene nanoribbon tunnel field effect transistor

Design of Energy Efficient Circuit Simulation

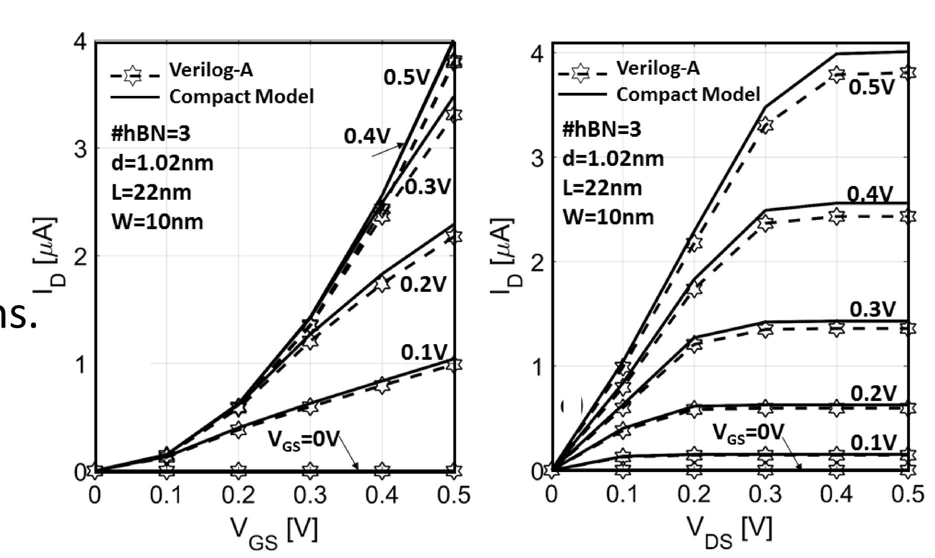
Process flow for incorporating compact models into circuit simulators

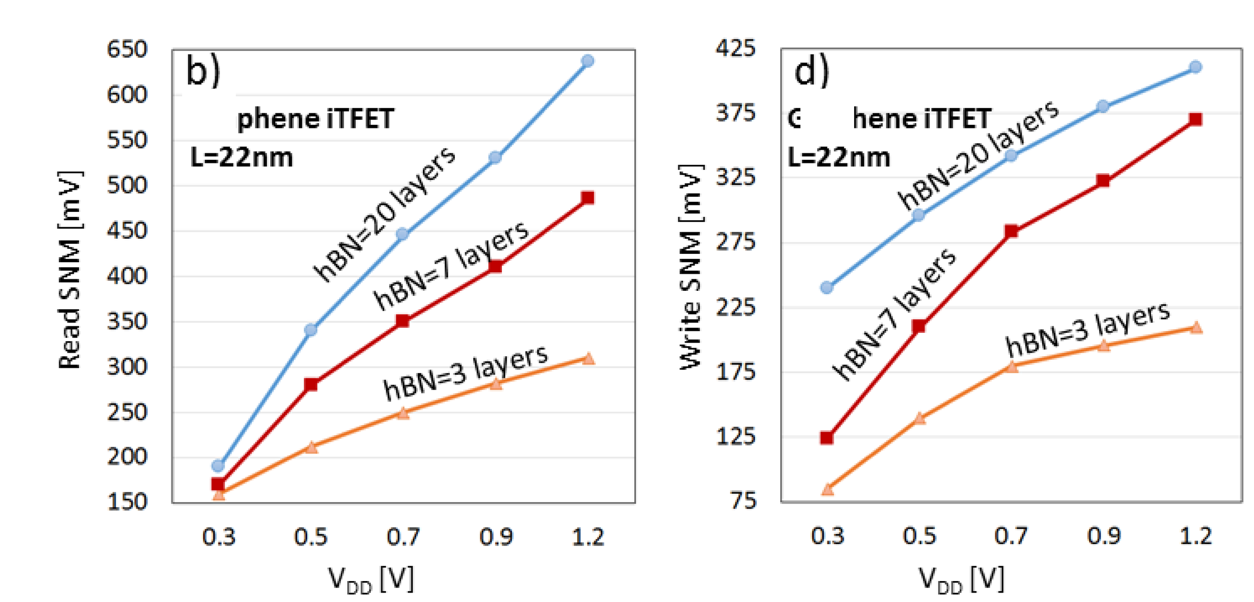


Performance Comparison and Static Random Access Memory (SRAM) Design

Features:

- Verilog-A simulated devices matches both physics based compact models and numerical simulations
- High read and write noise margins.
- Competitive performance than conventional FinFET and Si/Ge TFET





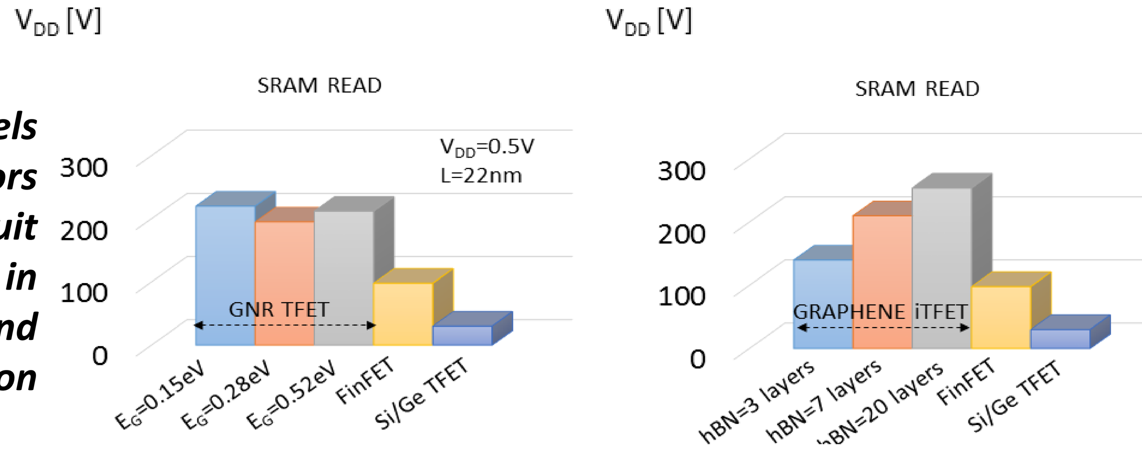


Fig. 7. Compact models of smart transistors based memory circuit design using Verilog-A in SPICE environment and performance evaluation and benchmarking.

Summary

- Energy efficient next generation smart transistors are studied from physics based compact models to their circuit level simulations.
- Promise of alternative current transport mechanism has been explored providing steeper sub-threshold slope than conventional planer TFET
- With continuous scaling of technology node following the Moore's law, energy efficient smart transistors are the demand of time.
- Compact model advances significant understanding from circuit design perspective.

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Acknowledgement

Part of the work of GNR TFET was conducted under the Airforce Research Lab (AFRL), Kirtland, NM under DoD contract FA9453-10-1-0002.